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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/029,679
Filing Date: December 21, 2001
Appellant(s): BOUCHARD ET AL.

William E. Lewis
Reg. No. 39,274
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 01/16/2007 appealing from the Office action mailed 06/14/2006

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,623,494	Rostoker et al.	08-1997
6,934,760	Westbrook et al.	08-2005
4,149, 243	Wallis	08-1979
4,593,357	Ostrand et al.	06-1986
6,058,114	Sethuram et al.	05-2000
6,483,839	Gemar et al.	11-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6 and 11-20 are rejected under 35 U.S.C 103(a) as being un-patentable over Rostoker et al. (U.S. 5,623,494) and further in view of Westbrook et al. (U.S. 6,934,760)

Regarding claim 1:

Rostoker discloses the invention substantially as claimed, including a system comprising:

First processing circuitry for performing a first function; first reassembly circuitry, associated with the first processing circuitry, for reassembling segments of received packets into reassembled packets, the segments to be reassembled being related to the first function; At least second processing circuitry for perform a second function; at least second reassembly circuitry, associated with the second processing circuitry, for reassembling segments of packets into reassembled packets: (Rostoker discloses Asynchronous Transfer Mode (ATM) interconnection

system includes a plurality of ATM terminal units connected with a plurality of host units for perform different or identical functions. In Rostoker's system, the plurality of "ATM terminal units" those share functionality with "first and second reassembly circuitries and their associated processing circuitries" as claimed can operate on a separate semi-conduct devices, and each of the ATM terminal unit can either perform assembly or reassembly ATM cells: abstract, lines 1-8;column 3, lines 37-45, 65-67; column 6, lines 32-67)

First memory circuitry, associated with the first processing circuitry, for storing the packets reassembled by the first reassembly circuitry; second memory circuitry, associated with the second processing circuitry, for storing the packets reassembled by the second reassembly circuitry: (Rostoker discloses each the ATM terminal unit includes a memory for storing segmented or reassembled ATM cells performed via the ATM terminal unit: column 3, lines 37-47, 53-55)

However, Rostoker does not explicitly disclose at least a portion of the same segments of packets reassembled by the first reassembly circuitry is reassembled into reassembled packets by the second reassembly circuitry

In analogous art, Westbrook discloses method for distributing re-sequencing of packets belonging to original packets stream in a compute or communication system, wherein the original packets stream is divided into a plurality of subsets of packets; each subset of packets are received at multiple "reassembly components" those share functionality with "reassembly circuitry" as claimed in order to produce a original larger packets, see (column 4, lines 1-47; abstract; figures 1B; 1C). For example, Westbrook discloses the re-sequencing of packets system (figures 1B; 1C) includes a plurality of "network input/output interfaces" those shares

functionality of reassembly components interoperate to each others; wherein each network input/output interface is capable to operate on either reassembly/and assembly packets, see (column 6, lines 55-60)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components with Rostoker's system in order to employ well-known technique into Rostoker's system for saving resources and development time, also to minimize bandwidth utilization, and to provide a higher rate packets transmission network, see (Westbrook: column 1, lines 37-60)

Regarding claim 2:

In addition to rejection in claim 1, Rostoker - Westbrook further discloses wherein the first processing circuitry, the first reassembly circuitry, the first memory circuitry, the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on the same integrated circuit: (Rostoker discloses the plurality of ATM terminals unit those share functionality with combination of the processing circuitry, the reassembly circuitry, the memory circuitry can be integrated into "a single chip/circuit" which shares functionality with "the same integrate circuit" as claimed: column 4, lines 20-25)

Regarding to claims 15 and 18:

Those claims are rejected under rationale of claim 1

Regarding claims 16 and 19:

Those claims are rejected under rationale of claim 2

Regarding claim 3:

In addition to rejection in claim 1, Rostoker - Westbrook further discloses the first processing circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry and the second memory circuitry are implemented on a second integrated circuit: (Westbrook discloses each subset of packets is continuously passed through "a plurality of reassembly components" for implementing reassembly the subset of packets; the examiner interprets reassembly component shares functionality with "combination of processing circuitry and its associated memory circuitry" as claimed, and further each reassembly component has characterizes of an integrated circuit itself: Westbrook: column 4, lines 1-47; abstract; figures 1B; 1C)

Regarding claims 17and 20:

Those claims are rejected under rationale of claim 3

Regarding claim 6:

In addition to rejection in claim 1, Rostoker - Westbrook further discloses network processor: (Rostoker discloses each of the ATM terminal unit includes a processor for segmenting and/or reassembling the ATM cells: abstract, lines 5-7)

Regarding claim 11:

In addition to rejection in claim 1, Rostoker-Westbrook further discloses a parsing circuitry: (this claimed feature inherently included in the Westbrook's system in order to be able to determining orders of packets for reassembling packets into original larger packets: column 4, lines 1-29)

Regarding claim 12:

In addition to rejection in claim 1, Rostoker - Westbrook further discloses ATM cells: (Rostoker's system may be implemented on reassembly ATM cells: abstract, lines 1-28)

Regarding claim 13:

In addition to rejection in claim 1, Rostoker - Westbrook further discloses switching device: (Rostoker discloses the ATM terminal unit can be processed at switching device: column 7, lines 65-67; column 8, lines 1-5)

Regarding claim 14:

In addition to rejection in claim 13, Rostoker - Westbrook further discloses network interfaces: (Westbrook's network input/output interfaces share functionality with reassembly circuits: figures 1B; 1C; column 6, lines 55-60)

Claim 4 is rejected under 35 U.S.C 103(a) as being un-patentable over Rostoker-Westbrook in view of Wallis (U.S. 4,149, 243)

Regarding to claim 4:

Rostoker - Westbrook discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein the first function and the second function are performed by an integrated circuit

However, in analogous art, Wallis's supervisory and task management system includes "a multiprocessor system" which shares functionality with "an integrated circuit" as claimed; therefrom, a first subunit processor implements first function, a second subunit processor implements second function. All the subunit processors performed under control of other on within the multiprocessor system: column 2, lines 28-52; column 3, lines 41-67; column 4, lines 1-7)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Wallis's ideas of all the subunit processors performed under control of other on within the multiprocessor system into Rostoker- Westbrook's system in order to improve the coordinations of dependent activities between subunit processors in a multiprocessing system for provide more flexibilities and to speed-up communication processes, see (Wallis: column 1, lines 57-67)

Claim 5 is rejected under 35 U.S.C 103(a) as being un-patentable over Rostoker-Westbrook in view of Ostrand et al. (U.S. 4,593,357)

Regarding to claim 5:

Rostoker - Westbrook discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein the first function and the second function are performed by different integrated circuits

However, in analogous art, Ostrand discloses a plurality of integrated circuits are housed in separate circuit board, see (column 5, lines 18-19)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Ostrand's ideas of a plurality of integrated circuits are housed in separate circuit boards with Rostoker - Westbrook's system in order to be easier to manage processing system, such as it's easier to adding/ removing/ modifying circuit boards separately to processing system: (Ostrand: column 5, lines 30-54)

Claim 7 is rejected under 35 U.S.C 103(a) as being un-patentable over Rostoker-Westbrook in view of Sethuram et al. (U.S. 6,058,114)

Regarding claim 7:

Rostoker - Westbrook discloses the invention substantially as disclosed in claim 6, but does not explicitly teach a packet classifying operation function

However, in analogous art, Sethuram discloses "a sorter" which is shared functionality with "classifier:" abstract, lines 1-15)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Sethuram's ideas sorting ATM cells according to prioritize and schedule in different manner into Rostoker- Westbrook's system in order to minimize bandwidth, memory utilization and to speed-up communication processing, see (Sethuram: column 6, lines 1-31)

Claims 8-9 are rejected under 35 U.S.C 103(a) as being un-patentable over Rostoker-Westbrook in view of Germar et al. (U.S. 6,483,839)

Regarding claim 8:

Rostoker - Westbrook discloses the invention substantially as disclosed in claim 1, but does not explicitly teach a traffic manager

However, in analogous art, Germar discloses a traffic manager: (abstract, lines 1-12)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Gemar's ideas of employing a traffic manager function into Rostoker- Westbrook's system in order to minimize bandwidth utilization, and further to provide a higher rate packets transmission system, see (Germar: abstract)

Regarding claim 9:

In addition to rejection in claim 8, Rostoker – Westbrook- Germar further discloses scheduling operation: (German discloses the traffic manager includes a scheduler: abstract)

(10) Response to Arguments

The examiner summarizes the various points raised by the appellant and addresses replies individually.

a) First, Appellant argues with respect to claim 1:

Rostoker fails to disclose the claimed features of: "the second reassembly circuitry, associated with the second processing circuitry, reassembly at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembly packets, the segments to be reassembled being related to a second function"

In reply to Appellant's arguments:

The examiner agrees; however, the examiner is not relying on Rostoker to meet this limitation of claim 1. Rather, the examiner is relying on Westbrook. Westbrook teaches a method for distributing re-sequencing of packets belonging to an original packets stream in a computer or communication system, wherein the original packets stream is divided into a plurality of subsets of packets; then "each subset of packets" (which shares functionality with "at least a portion of the same segments of packets" as claimed) are continuously received at "multiple reassembly components" (that share functionality with "the second reassembly circuitry and the first reassembly circuitry" as claimed) for reassembling the reassembled packets to produce the original larger packets, see (column 4, lines 1-47; abstract; figures 1B; 1C). Specifically, in the Westbrook's system, a plurality of network input/output interfaces also share functionality with reassembly components used to reassembly/or assembly ATM packets passed through them, see (figures 1B; 1C; column 6, lines 55-60). Thus, Westbrook meets this limitation of claim 1.

b) Second, Appellant arguesd with respect to claim 1:

Nowhere does Rostoker disclose at least a portion of the same of the same segments of packets reassembled by another one Note: It appears that this sentence is not complete.

In reply to Appellant's arguments:

The argument is addressed above in response to section a) above.

c) Third, Appellant argues with respect to claim 1:

Westbrook fails to disclose the claimed features "at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same".

In reply to Appellant's arguments:

This argument is also already addressed in sections a) above.

d) Fourth, ***Appellant argues with respect to claim 1:***

There is no suggestion to combine the Rostoker and the Westbrook references.

In reply to Appellant's arguments:

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components into Rostoker's system in order to save resources

and development time, to minimize bandwidth utilization, and to provide a higher rate packets transmitting system, see (Westbrook: column 1, lines 37-60) .

e) Fifth, Appellant argues with respect to claim 1:

The combination of the cited references do not disclose the first processing circuitry, the first reassembly circuitry, the first memory circuitry; the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on an integrate circuit.

In reply to Appellant's arguments:

Rostoke discloses a plurality of ATM terminal units are capable of reassembly / and assembly ATM cells, and several sets of ATM terminal units can be integrated into "an integrated circuit chip" (column 3, lines 34-46; column 4, lines 19-26).

f) Sixth, Appellant argues with respect to claim 1:

Rostker does not disclose the first processing circuitry, the first reassembly circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry, the second reassembly circuitry and the second memory circuit try are implemented on a second integrate circuit.

In reply to Appellant's arguments:

Westbrook discloses each subset of packets is continuously passed through a plurality of reassembly components for implementing reassembly on the subset of packets and each reassembly component has characterizes of an integrated circuit itself: (Westbrook: column 4, lines 1-47; abstract; figures 1B; 1C).

g) Last, Appellant argues with respect to claim 1:

Rostoker does not disclose claimed feature of: "the parsing circuitry...for parsing information from the received packets for use by the first reassembly circuitry and the second reassembly circuitry in respectively reassembling the packets".

In reply to Appellant's arguments:

Westbrook discloses the packets of original stream are marked with sequence numbers, timestamps, or other ordering indications which are distributed/ or sent over different paths and received by a plurality of reassembly components in order to produce original larger packets. Parsing circuitry is inherently included in Westbrook's system in order to parse orders of packets for reassembling packets back into the original larger packets (column 3, lines 37-59; column 4, lines 1-29).

h) ***Appellant argues with respect to claim 4:***

There is no suggestion to combine Rostoker, Westbrook and Wallis.

In reply to Appellant's arguments:

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Wallis's ideas of having all the subunit processors perform under control of other ones within the multiprocessor system with Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components into

Rostoker's system in order save resources and development time, to minimize bandwidth utilization, and to provide a higher rate packets transmitting system, (Westbrook: column 1, lines 37-60), and further to improve the coordinations of dependent activities between subunit processors in a multiprocessing system for faster communication processes (Wallis: column 1, lines 57-67).

i) ***Appellant argues with respect to claims 8-9:***

There is no suggestion to combine Rostoker, Westbrook and Gemar.

In reply to Appellant's arguments:

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Gemar's ideas of employing a traffic manager function with Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components into Rostoker's system in order to save resources and development time, to minimize bandwidth utilization, and to provide a higher rate packets transmitting system (Westbrook: column 1, lines 37-60; Germar: abstract).

j) ***Appellant argues with respect to claim 5:***

There is no suggestion to combine Rostoker, Westbrook and Ostrand.

In reply to Appellant's arguments:

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Ostrand's idea of having integrated circuits housed in separate circuit boards with Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components into Rostoker's system in order to save resources and development time, to minimize bandwidth utilization, and to provide a higher rate packets transmitting system (Westbrook: column 1, lines 37-60), and to easily manage processing systems (Ostrand: column 5, lines 30-54).

k) ***Appellant arguesd with respect to claim 7:***

There is no suggestion to combine Rostoker, Westbrook and Sethuram.

In reply to Appellant's arguments:

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Sethuram's ideas of sorting ATM cells according to

prioritt and schedule in a different manner with Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components into Rostoker's system in order to save resources and development time, to minimize bandwidth and memory utilization, and to provide a higher rate packets transmitting system (Westbrook: column 1, lines 37-60; Sethuram: column 6, lines 1-31).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusions

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Lan-Dai, Truong

05/09/2007

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